UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,118	07/09/2003	Vernon R. Brethour	ALER1560	2196

44654 7590 10/02/2006

SPRINKLE IP LAW GROUP
1301 W. 25TH STREET
SUITE 408
AUSTIN, TX 78705

EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,118	BRETHOUR ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The limitations of Independent claims 1 and 18, are directed to generating signals, and signal generation, i.e. number (waveform) manipulation is non-statutory subject matter. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 32-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 32 recites the limitation "said positive value and said negative value" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim since claim 28 does not mention any positive or negative values.

Dependent claims 33-43 are also rejected since they contain the same Limitation.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-3, 5-6, 18-20, 23, 28-30 are rejected under 35 U.S.C. 102(a) as being anticipated by Khaleghi et. al. (U.S. 6,618,430).

With respect to claim 1, Khaleghi et. al. disclose: selecting a code length (see Fig. 3A, 7 chips shown, column 4, lines 62-67, column 5, lines 1-4), said code length comprising a plurality of chips (Fig. 3 7 chips shown), wherein each chip of said plurality of chips is one of a non-zero value and a zero value (see Fig. 3, chips 1, 4, 7 are non-zero and chips 2,3,5,6 are zero, column 5, lines 1-20); and arraying said plurality of chips such that there is a plurality of said zero values within said plurality of chips and one or more said non-zero values is arrayed in accordance with a ruler (see column 5, lines 4-18, the Wx,y are spaced apart so that even when delays are present the chips from each signal will cross correlate to zero, see column 5, lines 8-14).

With respect to claim 2, all of the limitations of claim 2 are analyzed above in claim 1, and Khaleghi et. al. disclose: wherein said ruler is substantially orthogonal to time-shifted versions of said ruler (see 2nd example shown in Fig. 3A, if the non-zero signals in positions 1, 4, 7, are time-shifted to positions 2, 5, 8, that cross-correlation is substantially zero).

With respect to claim 3, all of the limitations of claim 3, are analyzed above in claim 2, and Khaleghi et. al disclose: wherein said chips are arrayed such that no two of said non-zero values are adjacent (see 2nd example of Fig. 3A).

With respect to claim 5, all of the limitations of claim 5, are analyzed above in claim 1, and Khaleghi et. al disclose: wherein said non-zero value is one of a positive value and a negative value (this would be implied, and Khaleghi et. al., discloses using spread Walsh codes (where Walsh codes have values of –1 +1)).

With respect to claim 6, all of the limitations of claim 6 are analyzed above in claim 5, and Khaleghi et. al. disclose: wherein said ruler is substantially orthogonal to time-shifted versions of said ruler (see 2nd example shown in Fig. 3A, if the non-zero signals in positions 1, 4, 7, are time-shifted to positions 2, 5, 8, that cross-correlation is substantially zero).

With respect to claim 18, Khaleghi et. al., disclose: defining said set such that all of said communications signal codes in said set have a code length (see Fig. 3A, arbitrary number of chips comprise the code) , said code length comprising a plurality of chips, each of said chips having a value, said value being one of a positive value, a negative value and a zero value (Fig. 3A, see zero values in chip 2, and positive or negative (depending on the Walsh code used, column 4, lines 28-32)) ; arraying said chips such that at least one said positive value and at least one said negative value is placed in accordance with a ruler (Fig. 3, non-zero chip values are spaced apart, see column 5, lines 8-15, so that even if delays are present the chips still correlate to zero, i.e. are orhtogonal) said ruler being substantially orthogonal to all time-shifted versions of said ruler, and such that at least one of said chips has a zero value (see column 5, lines 8-15, so that even if delays are present the chips still correlate to zero, i.e. are orthogonal); and arraying said chips such that said at least one positive value and said at least one negative value are placed in accordance with a pattern, said pattern being from a family of binary patterns wherein each pattern within said family of patterns is substantially orthogonal to substantially all time-shifted versions of each other pattern within said family of patterns (see Fig. 3A, non-zero chips are spread walsh patterns, and Walsh codes are orthogonal codes).

With respect to claim 19, all of the limitations of claim 19 are analyzed above in claim 18, and Khaleghi et. al., disclose: wherein said ruler belongs to a family of rulers wherein each ruler within said family is substantially orthogonal to

each other ruler within said family of rulers (see column 5, lines 18-21, where it is understood that the non-zero valued chips can be spaced further apart (2,3, or any other number of zero chips placed between the non-zero chips and this would correspond to the family of rulers, and depending on the number of zero see Fig. 3B for example there can be no cross correlation between the non-zero chips).

With respect to claim 20, all of the limitations of claim 20 are analyzed above in claim 19, and Khaleghi et. al., disclose: wherein said code length is 26 chips (embodiments shown in Fig. 3 show an arbitrary number of chips, i.e. they can be 26 chips).

With respect to claim 23, all of the limitations of claim 23, are analyzed above in claim 19, and Khaleghi et. al disclose: wherein said chips are arrayed such that no two of said non-zero values are adjacent (see 2nd example of Fig. 3A).

With respect to claim 28, Khaleghi et. al. disclose: a radio transmitter (Fig. 3A signals are transmitted signal, and it is understood that these signals are generated in a transmitter); and a radio receiver (Fig. 11, column 5, lines 49-53), said transmitter and said receiver employing a communications signal having a code length, said code length comprising a plurality of chips, wherein each chip of said plurality of chips is one of a non-zero value and a zero value (see

transmitted signal shown in Fig. 3A, column 5, lines 7-21), and wherein said chips are arrayed such that there is a plurality of zero values within said plurality of chips and one or more said non-zero values is arrayed in accordance with a ruler (column 5, lines 7-21, the non-zero valued chips are spaced apart so that their cross-correlation properties are retained).

With respect to claim 29, all of the limitations of claim 29 are analyzed above in claim 28, and claim 29 is analyzed similarly to claim 2 above.

With respect to claim 30, all of the limitations of claim 30 are analyzed above in claim 29, and claim 30 is analyzed similarly to claim 3.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-2, 5-9, 12-15, 18-22, 28-29, 32-33, 38, are rejected under 35 U.S.C. 102(b) as being anticipated by Hostetter et. al., (U.S. 5,450,395).

With respect to claim 1, Hostetter et. al. disclose: selecting a code length (see Fig. 5, size of transmissions "121", "122", "123", "124" is 1023 chips, column 12, lines 44-49) said code length comprising a plurality of chips (1023 chips,

column 12, lines 46-47), wherein each chip of said plurality of chips is one of a non-zero value and a zero value (see Fig. 5, for example transmission "121"); and arraying said plurality of chips such that there is a plurality of said zero values within said plurality of chips and one or more said non-zero values is arrayed in accordance with a ruler (see Fig. 5, transmission "121", column 12, lines 41-44, where CPMMA stands for code position modulated multiple access, see also column 13, lines 28-30, where the ruler determines the starting chip position, see also table VII shown in column 13-14).

With respect to claim 2, all of the limitations of claim 2 are analyzed above in claim 1, and Hostetter et. al. disclose: wherein said ruler is substantially orthogonal to time-shifted versions of said ruler (Fig. 5, time shifting the position of the ones of transmission "121" is substantially orthogonal to the original pattern of ones).

With respect to claim 5, all of the limitations of claim 5 are analyzed above in claim 1, and Hostetter et. al. disclose: wherein said non-zero value is one of a positive value and a negative value (see Fig. 5, transmission 121 includes "ones").

With respect to claim 6, all of the limitations of claim 6, are analyzed above in claim 5, and Hostetter et. al. disclose: wherein said ruler is substantially orthogonal to all time-shifted versions of said ruler (Fig. 5, time shifting the

position of the ones of transmission "121" is substantially orthogonal to the original pattern of ones).

With respect to claim 7, all of the limitations of claim 7 are analyzed above in claim 6, and Hostetter et. al. disclose: wherein said step of arraying said plurality of chips further comprises the step of arraying at least one said positive value (maximal length code (MLC) also known as PN code are used in transmission 121, etc).

With respect to claim 8, all of the limitations of claim 8 are analyzed above in claim 7, and Hostetter et. al. disclose: wherein said pattern is selected from a family of patterns (maximal length (PN codes) patterns are used).

With respect to claim 9, all of the limitations of claim 9 are analyzed above in claim 8, and wherein said family of patterns wherein any pattern within said family of patterns is substantially orthogonal to substantially all time-shifted versions of any other pattern within said family of patterns (MLC or PN codes are orthogonal).

With respect to claim 12, all of the limitations of claim 12 are analyzed above in claim 5, and claim 12 is analyzed similarly to claim 9 above.

With respect to claim 13, all of the limitations of claim 13 are analyzed above in claim 12, and claim 13 is analyzed similarly to claim 7 above.

With respect to claim 14, all of the limitations of claim 14, are analyzed above in claim 13, and claim 14 is analyzed similarly to claim 8 above.

With respect to claim 15, all of the limitations of claim 15 are analyzed above in claim 14, and claim 15 is analyzed similarly to claim 9 above.

With respect to claim 18, Hostetter et. al. disclose: defining said set such that all of said communications signal codes in said set have a code length (column 12, lines 44-49, 1023 chips or other size), said code length comprising a plurality of chips, each of said chips having a value (see Fig. 5, chips Cn are either "0" or "1"s, column 13, lines 1-10) , said value being one of a positive value, a negative value and a zero value (positive or zero values as shown in Fig. 5); arraying said chips such that at least one said positive value and at least one said negative value is placed in accordance with a ruler (the ruler defines the starting chip, see column 13-14 table VII and an example of the ruler would be the starting chip 2, which does not correlate with time shifted version of itself) said ruler being substantially orthogonal to all time-shifted versions of said ruler, and such that at least one of said chips has a zero value (Fig. 5 shows chips with zero values); and arraying said chips such that said at least one positive value and said at least one negative value are placed in accordance with a pattern,

said pattern being from a family of binary patterns wherein each pattern within said family of patterns is substantially orthogonal to substantially all time-shifted versions of each other pattern within said family of patterns (Fig. 5, column 13, lines 1-11, the family of patterns is the MLC codes and these codes are orthogonal).

With respect to claim 19, all of the limitations of claim 19 are analyzed above in claim 18, and claim 19 is analyzed similarly to claim

With respect to claim 20, all of the limitations of claim 20, are analyzed above in claim 19, and Hostetter et. al. disclose: wherein said code length is 26 chips.

With respect to claim 21, all of the limitations of claim 21 are analyzed above in claim 20, and Hostetter et. al. disclose: wherein said family of rulers comprises one ruler where said one ruler comprises seven non-zero value chips.

With respect to claim 22, all of the limitations of claims 21 are analyzed above in claim 21, and Hostetter et. al. disclose: wherein said family of patterns is comprised of eight patterns.

With respect to claim 28, Hostetter et. al. disclose: a radio transmitter (see Fig. 3, receveiver/transmit unit of the invention); and a radio receiver (see

Fig. 3 as above), said transmitter and said receiver employing a communications signal having a code length (column 12, section "code time slots", lines 44-49), said code length comprising a plurality of chips (see fig. 5, transmissions include chips), wherein each chip of said plurality of chips is one of a non-zero value and a zero value (see Fig. 5), and wherein said chips are arrayed such that there is a plurality of zero values within said plurality of chips and one or more said non-zero values is arrayed in accordance with a ruler (column 13, lines 2-27, and table VII rules).

With respect to claim 29, all of the limitations of claim 29 are analyzed above in claim 28, and claim 29 is analyzed similarly to claim 2 above.

With respect to claim 32, all of the limitations of claim 32 are analyzed above in claim 28, and Hostetter et. al. disclose: wherein said positive value and sadi negative value correspond to an amplitude of an impulse (see Fig. 5, a chip with a value of "1" out of the 1023 chips is considered as an impulse).

With respect to claim 33, all of the limitations of claim 33 are analyzed above in claim 32, and claim 33 is analyzed similarly to claim 18 above.

With respect to claim 38, all of the limitations of claim 38 are analyzed above in claim 32, and claim 38 is analyzed similarly to claim 18 above.

Allowable Subject Matter

9. Claims 30-31, 34-37, 39-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Walthall (U.S. 5,353,303) disclose: a method of increasing the bit rate of a data link by using a specific arrangement of chip code patterns.

McCorkle et. al., (U.S. 2003/0161411) disclose: an UWB system using orthogonal wavelets.

Soo et. al., "Asynchronous multirate optical wireless PPM-CDMA in an indoor non-directed diffuse channel", Electronics Letters, 1997 disclose: a pulse position modulation PP-CDMA system.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
9/21/2006

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER